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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/872,796	06/01/2001	Craig L. Stevens	10001.000600 (NVLS 379)	4156

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EXAMINER

KIELIN, ERIK J

ART UNIT	PAPER NUMBER
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2813

DATE MAILED: 05/19/2003

18

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/872,796

Applicant(s)

STEVENS ET AL.

Examiner

Erik Kielin

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-- The MAILING DATE of this communication appears on the cover sheet with the corresponding address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 13 March 2003.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-13, 17 and 19-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-13, 17 and 19-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 June 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All   b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 15.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

### DETAILED ACTION

This action responds to the Amendment (Paper No. 17) and the IDS (Paper No. 15) each filed 13 March 2003.

#### *Drawings*

Examiner acknowledges Applicant's statement in the response filed 13 March 2003 (Paper No. 17), in the last paragraph on p. 4 that the drawings are not prior art with respect to 35 USC 102. Accordingly, the objection is withdrawn.

#### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-13 and 17, 19-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Independent claims 1 and 17 were amended to recite the limitation that the load lock chamber has "only a single wafer support." This is unclear because it appears that the intent of the specification is that the load lock chamber has --only **one** single-wafer support-- while, as presently written, the limitation suggests that there exists nothing else in the load lock chamber which is not supported by the specification.

For the purpose of patentability the claims will be considered in accordance with the specification, as just noted.

The remaining claims are rejected for depending from the above rejected claims 1 and 17.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-13 and 17, 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,251,759 B1 (**Guo et al.**) in view of US 6,270,582 B1 (**Rivkin et al.**).

Regarding independent claims 1 and 17, **Guo** discloses a wafer processing system comprising:

a load lock 114 (Fig. 1);

a transport module having a load chamber 113 (called "buffer chamber" in **Guo**), a transfer chamber 101, and a pass-through chamber 122 (additionally called "transition chambers" in **Guo** col. 4, line 19) located between the load chamber and the transfer chamber, the load chamber being coupled to the load lock;

an intermediate process module 124 (called "transition chambers" in **Guo** col. 4, line 19) coupled to the load chamber and the transfer chamber (as further limited by instant claim 20);

a first set of process modules 116, 118, 121 coupled to the load chamber;

a second set of process modules 104, 106, 108, 110 coupled to the transfer chamber.

**Guo** does not indicate if the load lock is a single-wafer load lock having a single-wafer, water-cooled pedestal (as further limited by instant claims 8 and 19).

**Rivkin** teaches only one single-wafer load lock (title) for a multi-chamber semiconductor wafer process module having water-cooled, single-wafer pedestal 136, wherein the cooling unit

is integrally formed with the pedestal and the load lock chamber (Fig. 3; col. 6, lines 1-4, lines 37-47). While it is noted that Figs. 3 and 4 in **Rivkin** show two wafer holders **140, 142** (Fig. 3), **182, 184** (Fig. 4), **Rivkin** is not limited to these exemplary embodiments as the claims make clear. Claim 8 in **Rivkin** recites the limitation, “wherein the wafer holder includes a *maximum* of two wafer supports for supporting a maximum of two wafers.” (Emphasis added.) Since “two” is stated to be the “maximum” number of wafer holders then, this claim implicitly indicates that there may be only one single wafer holder. Additional support comes from the **Rivkin** independent claim 33 as compared to claim 39. Claim 33 claims “a wafer holder” (emphasis added) while claim 39, which depends from claim 33 indirectly, claims “a **second** wafer holder” (emphasis added). Clearly, only one wafer holder is claimed in claim 33 --made especially clear by dependent claim 39. Moreover, at col. 9, lines 28-30, **Rivkin** states, “Another advantage of a load lock chamber **108** that *only holds a single wafer* is that the wafer is accessible to a wafer orienter.” (Emphasis added.) For all these reasons, **Rivkin** at least implicitly, if not expressly teaches the limitation of only one single-wafer holder.” Note “[I]n considering the disclosure of a reference, it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom.” *In re Preda*, 401 F.2d 825, 826, 159 USPQ 342, 344 (CCPA 1968) See also *In re Lamberti*, 545 F.2d 747, 750, 192 USPQ 278, 280 (CCPA 1976).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use the single-wafer load lock of **Rivkin**, in the process system of **Guo** to enable additional processing not typically provided in a load-lock, as is taught to be beneficial in **Rivkin** (Abstract and Summary of Invention).

Regarding claims 2, **Guo** shows process module **118** connected to the load chamber 113 (the first set of process modules) may be a pre-clean module (col. 4, line 7).

Regarding claims 3 and 4, **Guo** shows process module **121** connected to the load chamber 113 (the first set of process modules) may be a physical vapor deposition (PVD) or chemical vapor deposition (CVD) module (col. 4, lines 49-52).

Regarding claim 6, **Guo** shows process module **104** connected to the transfer chamber 101 (the second set of process modules) is a chemical vapor deposition (CVD) module (col. 4, lines 64-66).

Regarding claims 10, 11, and 21, **Guo** discloses that it is known for the intermediate process module **122** to be configured as either a cooling station or a pre-clean module (col. 1, 45-48; col. 4, line 47).

Regarding claim 12, **Guo** shows the intermediate process module **124** is configured as a PVD chamber.

Regarding claims 5, 7, 9, and 13, **Guo** does not specifically indicate that the second set of process modules (those on the transfer chamber **101**) include a pre-clean module (claim 5) or a PVD module (claim 7), or that the intermediate process module **122**, **124** may be configured as a degas module (claim 9) or a CVD module (claim 13). Note however, that **Guo** teaches the benefits of configuring one of the intermediate chambers **122**, **124** as a PVD module (col. 3, lines 43-50). Additionally, **Guo** teaches that the ordering of process modules is “illustrative” (col. 3, lines 60-63), and that cluster tools include a variety of ordered tools depending upon the process being performed (col. 1, lines 30-48), and also that metallization cluster tools include CVD, PVD, pre-clean and degas modules, among others (col. 2, lines 34-59 and through out the

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specification and figures). This suggests to one of ordinary skill in the art that the arrangement is a matter of design choice to best suit a given processing steps to be performed in a semiconductor wafer. Moreover, it has been held that mere rearrangement of parts is evidence of obviousness. *In re Kuhle*, 526 F.2d 553, 188 USPQ 7 (CCPA 1975) (the particular placement of a contact in a conductivity measuring device was held to be an obvious matter of design choice).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to have a pre-clean module or PVD module in the second set of process modules and to have a degas and pre-clean modules as intermediate modules, in order to optimize the process throughput for a given process, as taught by **Guo** and according to precedent. Moreover, Applicant indicates that virtually any arrangement of process modules is possible, thereby teaching away from the criticality of any specific arrangement in the processing system.

### ***Response to Arguments***

5. Applicant's arguments filed 13 March 2003 have been fully considered but they are not persuasive.

Applicant amended the independent claims 1 and 17 to claim that only a single wafer support is provided in the load lock chamber and that Guo and Rivkin --particularly Rivkin-- does not teach this. Examiner disagrees because at least the claims of Rivkin are not so limited to those embodiments shown in Figs. 3 and 4. Claim 8 in **Rivkin** recites the limitation, "wherein the wafer holder includes a *maximum* of two wafer supports for supporting a maximum of two wafers." (Emphasis added.) Since "two" is stated to be the "maximum" number of wafer holders then, this claim implicitly indicates that there may be only one single wafer holder. Additional

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support comes from the **Rivkin** independent claim 33 as compared to claim 39. Claim 33 claims “a wafer holder” (emphasis added) while claim 39, which depends from claim 33 indirectly, claims “a **second** wafer holder” (emphasis added). Clearly, only one wafer holder is claimed in claim 33 --made especially clear by dependent claim 39. Moreover, at col. 9, lines 28-30, **Rivkin** states, “Another advantage of a load lock chamber **108** that *only holds a single wafer* is that the wafer is accessible to a wafer orienter.” (Emphasis added.) For all these reasons, **Rivkin** at least implicitly, if not expressly teaches the limitation of only one single-wafer holder.”

Applicant argues that the Rivkin two wafer support prevents the ability of Rivkin to have an integral cooling unit. This feature is shown in Fig. 3 and discussed in col. 6, lines 37-47 in Rivkin. Accordingly, this argument is moot.

### *Conclusion*

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 5,199,483 (**Bahng**) discloses a cooling system for wafers (Abstract).

US 5,281,320 (**Turner et al.**) teaches that the load lock volume should be minimized to accommodate a single wafer in order to reduce the amount of pumpdown required for the load lock (col. 7, lines 112-16).

US 5,789,878 (**Kroeker et al.**) states,

“Modern semiconductor processing systems include cluster tools that integrate a number of process chambers together in order to perform several sequential processing steps without removing the substrate from the highly controlled processing environment. These chambers may include, for example, degas chambers, substrate pre-conditioning chambers, cooldown chambers, transfer chambers, chemical vapor deposition chambers, physical



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vapor deposition chambers, and etch chambers. The combination of chambers in a cluster tool, as well as the operating conditions and parameters under which those chambers are run, are selected to fabricate specific structures using a specific process recipe and process flow.

Once the cluster tool has been set up with a desired set of chambers and auxiliary equipment for performing certain process steps, the cluster tool will typically process a large number of substrates by continuously passing them, one by one, through the same series of chambers or process steps. The process recipes and sequences will typically be programmed into a microprocessor controller that will direct, control and monitor the processing of each substrate through the cluster tool.” (See col. 9, line 51 to col. 10, line 10.)

Moreover, **Kroeker** shows that the second set of process modules on the transfer chamber include both CVD and PVD. This provides suggestion to one of ordinary skill to order the first set, second set, intermediate, and pass-through modules for whatever processing best suits the sequence of the steps.

US Patent application 2001/0041122 A1 (**Kroeker**) teaches a single wafer load lock. (Abstract).

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37


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CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 703-306-5980. The examiner can normally be reached on 9:00 - 19:30 on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 703-308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

  
Erik Kielin  
May 17, 2003